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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,551	09/16/2003	William J. Borland	EL0496 US NA	2580

23906 7590 03/28/2005

E I DU PONT DE NEMOURS AND COMPANY
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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

N·A

Office Action Summary	Application No.	Applicant(s)	
	10/663,551	BORLAND ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1-15-04, 2-4-04, 5-17-04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7-9, 11-15, 17-20, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,395,996 (Tsai).

Tsai discloses, referring primarily to figure 2, a printed wiring board, comprising: a first circuit conductor (164) extending through at least a part of the printed wiring board; a second circuit conductor (162) extending through at least a pad of the printed wiring board; and a plurality of stacked inner layer panels, wherein at least one of the inner layer panels comprises: a first electrode (130A) formed from a foil and having a termination, wherein the first circuit conductor is coupled to the first electrode at the termination of the first electrode, and wherein the first electrode termination is within a footprint of the first electrode; at least one dielectric (135) disposed over the first electrode; and a second electrode (140A) spaced from the first electrode and having a termination, wherein the second electrode, the first electrode, and the dielectric form a capacitor (see col. 4, lines 10-30), and wherein the second circuit conductor is coupled to the second electrode termination [**claim 1**], wherein the first circuit conductor extends

through the dielectric [**claim 2**], wherein: the second electrode termination is within a footprint of the second electrode; and the second circuit conductor extends through the dielectric [**claim 3**], the inner layer comprising a laminate material (145, 125) disposed over the first and second electrodes and over the dielectric, wherein the first circuit conductor extends through the laminate material [**claim 4**], wherein the second circuit conductor extends through the laminate material [**claim 5**], wherein the first electrode has a first component side that contacts the dielectric, and a second side opposite to the first side, and wherein the first circuit conductor extends from the second side of the first electrode [**claim 7**], wherein the termination of the second electrode is within a footprint of the second electrode [**claim 8**], the inner layer comprising; a laminate material (125) disposed over the second side of the first electrode, wherein the first circuit conductor extends through the laminate material and the second circuit conductor extends through the laminate material [**claim 9**].

Similarly, Tsai discloses, referring primarily to figure 2, a method of making a printed wiring board, comprising: forming a plurality of stacked inner layer panels (see col. 3, lines 30-45), wherein forming at least one of the inner layer panels comprises: providing a metallic foil (130A); forming a dielectric (135) over the metallic foil; forming a first electrode from the metallic foil, the first electrode having a termination located within a footprint of the first electrode; and forming a second electrode (140A) over the dielectric, the second electrode having a termination, wherein the first electrode, the second electrode, and the dielectric form a capacitor (see col. 3, lines 45-60), forming a first circuit conductor (164), wherein the first circuit conductor extends through at least a

portion of the printed wiring board and contacts the first electrode termination; and forming a second circuit conductor (162), wherein the second circuit conductor contacts the second electrode termination and extends through at least a portion of the printed wiring board [**claim 11**], wherein forming a dielectric comprises: forming a dielectric having a through-hole (105, figure 3) circuit conductor extending through the through-hole [**claim 12**] wherein: the second electrode termination is within a footprint of the second electrode; ad forming a second circuit conductor comprises forming a conductive via that extends through the dielectric [**claim 13**], wherein forming the inner layer panel comprises; forming a laminate material (145, 125) over the first and second electrodes and over the dielectric [**claim 14**], wherein: forming the first circuit conductor comprises forming a conductive via through the laminate material; and forming the second circuit conductor comprises forming a conductive via through the laminate material [**claim 15**], wherein forming the inner layer panel comprises; providing a laminate material (135) and laminating the metallic foil (130) to the laminate material before forming the first electrode (see figure 3) [**claim 17**], wherein the first electrode has a first component side that contacts the dielectric, and a second side opposite to the first side, wherein forming the first circuit conductor comprises: forming the first circuit conductor to extend from the second side of the first electrode [**claim 18**], wherein: the second electrode termination is within the footprint of the second electrode; and forming the inner layer panel comprises forming a laminate material (125) over the second side of the first electrode [**claim 19**], wherein: forming a first circuit conductor comprises forming a conductive via through the laminate material; and forming a

second circuit conductor comprises forming a conductive via through the laminate material [**claim 20**], wherein forming the inner layer panel comprises; providing a laminate material; and laminating the metallic foil (130) to the laminate material before forming the first electrode [**claim 22**].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 6, 10, 16, 21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai.

Tsai discloses the claimed invention as described above except Tsai does not specifically disclose a third electrode spaced from the second electrode and electrically connected to the first electrode, and wherein the first electrode, the second electrode, the dielectric, and the third electrode form a capacitor [**claims 6, 10, 16, 21**]. However, Tsai teaches that the board may comprise multiple built in capacitors (see col. 2, lines 30-35). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to form a second built in capacitor substantially similar to the first capacitor, having a third electrode connected to the first via (and thus electrically connected to the first electrode). The motivation for doing so would have been to better filter the noises (see col. 3, lines 15-25)

Similarly, Tsai discloses the claimed invention as described above except Tsai does not specifically state forming a third circuit conductor through at least two of the joined inner layer panels; and incorporating the joined inner layer panels into the printed wiring board [**claim 23**]. However, Tsai teaches via a prior art device (figure 1) that it is known in the art to penetrate conductive vias separate from capacitor vias, through panel layer. Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to form a third conductive via through the device of Tsai.

The motivation for doing so would have been to allow for signal communication between the two outer signal layers.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents disclose PCBs having embedded capacitors:

US 6,005,197 Kola et al.,

US 6,021,050 Ehman et al.,

US 6,153,290 Sunahara,

US 6,597,056 Muramatsu et al..

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

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